

# Schottky LSI, Inc <sup>TM</sup>

## Executive Brief

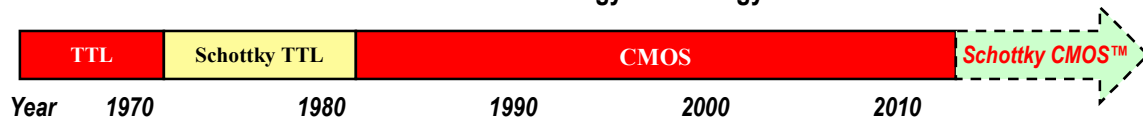
### Schottky CMOS<sup>TM</sup> Circuit Technology Disruptive Advantages in Speed, Power & Cost

**Introduction** | Schottky CMOS<sup>TM</sup> is a novel, patented circuit technology that offers our customers a quantum leap in power, performance and cost advantages for any given CMOS Semiconductor Process Node.

Our Schottky CMOS<sup>TM</sup> Circuits can run more than 100% faster and *simultaneously* burn 60%+ less power than equivalent CMOS Circuits. In addition our area is 60%+ smaller. Our Technology is process node agnostic and runs on any standard CMOS process, including FinFET. We enable an IC using 28 nm process to win against a 20 nm IC, or a 20 nm IC to win against a 16 nm FinFET IC. We can also enable 16 nm FinFET to win against a 10 nm FinFET.

The below graph shows the progression of Circuit Innovation over the last 50 years. In 1970 Schottky TTL, with superior speed, power & cost advantages, displaced TTL. The result was the relentless shrinking of transistors continued on Schottky TTL instead of TTL. In 1980 the more advantageous CMOS Circuits displaced Schottky TTL. For the next 30 years, the Industry has been shrinking CMOS. It is time for a new circuit innovation, and we believe it is our Schottky CMOS<sup>TM</sup> Circuit Technology that will replace CMOS Circuits going forward,

#### Circuit Technology Chronology



**Value Proposition** | Our Schottky CMOS<sup>TM</sup> Circuit Technology will give IC Companies winning advantages in better speed, power and cost, and will enable older foundries to compete against newer foundries.

**Product & Markets** | This Technology can add winning advantages to Foundries and IC companies in Big Data, Mobile Markets and to ICs in general, including flash, memory, microprocessor, FPGAs, ASICs as well as analog.

**Competition** | There are no known competitors. The Company believes this is a window of opportunity for the early adopters of this technology to win against their competitors.

**Risk** | Circuit Design Risk is much less than the new 3 dimension FinFET with molecular size transistors.

**Business Model** | The Company 's business model is to license the technology to fabless IC companies, to foundries and IDM companies, Our monetization model includes NRE for services, up-front licensing fees and royalty.

#### Founders & Management

**Ven L. Lee, Co-Founder, President & CEO**

*Prior Co-Founder & CEO nDSP/Sold to Pixelworks, Prior VP/GM LSI Logic Corp*

**Augustine Chang, Co-Founder & CTO. Inventor of Schottky CMOS<sup>TM</sup>**

*Inventor of Industry wide technologies such as Schottky TTL, Oxide Isolation. IBM Inventor*

**Dan Tuchler, VP Marketing and Product management,**

*VP of IBM Blade Network Technologies. Senior executive of Mellanox, Vyatta, Blade, and Brocade*

**Thomas Dockery, Business Development Executive**

*VP Sales of eSilicon, Director of Mobile Markets at Synaptics*

**Corporate Attorney:** Wilson Sonsini Goodrich & Rosati LC, Palo Alto, CA, US